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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,841	12/17/2003	Charles P. Thacker	003797.00689	5432

28319 7590 01/11/2007

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,841	THACKER, CHARLES P.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 8-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 1 December 2006. Claims 1-4 and 8-21 are pending. Claims 5-7 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4 and 8-21 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 3-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3 recited the limitation of "a second array of sensing loops each coupled between the processor and a SECOND potential node." This is not enabled because claim 1 to which claim 3 depends already states that the second array is coupled between the processor and the first potential node. The specification provides no explanation as to how the sensing loop can be coupled between the processor and a first potential node and a second potential node at the same time, and instead only shows that the sensing loops are selectively connected to the processor and ground. The examiner notes that the only way that this claim is enabling is if the first potential node and the second potential node are equal, which would mean that this claim is not further limiting.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanami et al. (US 4,878,553) in view of Tamura et al. (US 4,571,454).

Regarding claim 1, Yamanami et al. disclose an electronic digitizer sensor coupled to a processor comprising:

a first array of sensing loops (Figure 1, item 10) each coupled between the processor and a first node, each sensing loop in the first array being selectively connectable to the processor and further being selectively connectable to the first node (Figure 1 shows processing device 70, where each sensing loop 11-1 through 11-48 is

coupled between the processor through the transmitting device at the node represented between switches 23 and 31 being selectively connected by switch 23, and are coupled to a first node which is the node between switches 24 and 32 being selectively connected by switch 24.); and

a second array of sensing loops each coupled between the processor and the first node, each sensing loop in the second array being selectively connectable to the processor and further being selectively connectable to the first node (Please refer to the description for the first array of sensing loops above and Figure 9 and column 10, lines 28-63 which explain that each the x and y layers shown as 81 and 82 respectively each have the configuration as that shown in Figure 1.);

wherein the first array of sensing loops are each disposed at a first level but not at a different second level (Figure 9 shows that the x level loop would be at a level 81 and not at the level 82.), and

wherein the second array of sensing loops are each disposed at the second level but not the first level (Figure 9 shows that the y level loop would be at a level 82 and not at the level 81.).

Yamanami et al. fail to teach wherein the electronic digitizer sensor comprises a substrate, where the first and second sensing loops are each disposed on first and second levels of the substrate respectively, and wherein the first node is a first potential node.

Tamaru et al. disclose wherein a electronic digitizer sensor comprises a substrate, where first and second sensing electrodes are each disposed on first and

second levels of the substrate respectively (Figure 7 and column 5, lines 30-63 explain that the position determining plate 10, which the examiner considers a substrate, has y electrodes on a first transparent insulating layer 11 of the substrate and x electrodes on a second transparent insulating layer 12 of the substrate.), and also disclose wherein the first and second arrays of sensing electrodes are selectively connected to a first potential node (Figure 7 shows that each of the electrodes is selectively connectable to either a ground or voltage source.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the sensing loops taught by Yamanami et al. on different levels of a substrate and each of them selectively connectable to a first potential node as taught by Tamaru et al. in order to be able to ground the sensing loops not being used for detection to reduce noise coupling of the sensing loops.

Regarding claim 2, Yamanami et al. and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 1.

Tamaru et al. also disclose a digitizer sensor wherein the first potential node is a ground node (Figure 7 shows that the node A is a ground node.).

Regarding claim 3, please refer to the rejection of claim 1, and furthermore Tamaru et al. shows in Figure 7 that the second sensing array is also coupled to a second potential node B connected to +Vcc.

Regarding claim 4, Yamanami et al. and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 3.

Tamaru et al. also disclose wherein at least one of the first and second levels of the substrate are a surface of the substrate (Column 5, lines 30-63 explain that the position determining plate, i.e. the substrate as explained in the rejection of claim 1, comprises of a first transparent payer 11 which has the y electrodes of the surface, meaning that the y array is on a level which is one of the surfaces of the substrate.).

Regarding claim 8, this claim is rejected under the same rationale as claim 1.

Regarding claim 9, Yamanami et al. and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 8.

Tamaru et al. also disclose an electromagnetic digitizer sensor wherein the first sensing loops are arranged in a comb-like pattern and the second sensing loops are arranged in a comb-like pattern (Fig. 1, where the X electrodes and the Y electrodes are both in a "comb-like pattern").

Regarding claim 10, Yamanami et al. and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 8.

Tamaru et al. also disclose an electromagnetic digitizer sensor integrated with a display (see col. 1, lines 6-7).

9. Claims 11-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanami et al. (US 4,878,553) in view of Blesser (US 4,694, 124) and further in view of Tamura et al. (US 4,571,454).

Regarding claim 11, Yamanami et al. disclose an electromagnetic digitizer sensor coupled to a processor, comprising:

a first plurality of sensing traces electrically coupled in parallel between the processor and a node (Figure 1 shows processing device 70, where each sensing loop 11-1 through 11-48 is coupled between the processor through the transmitting device at the node represented between switches 23 and 31 being selectively connected by switch 23, and are coupled to a node between switches 24 and 32 being selectively connected by switch 24.);

a first switch coupled between the first plurality of sensing traces and the processor (Figure 1 shows a first switch 23.); and

a second plurality of switches each coupled between the first plurality of sensing traces and the node (Figure 1 shows a second switch 24.).

Yamanami et al. fail to teach a first node in the middle of the sensing loop creating a plurality of traces electrically coupled between a processor and said first node, and further creating a plurality of traces electrically coupled between the second node and the first node.

Blesser discloses digitizing tablet comprising a first node in the middle of a sensing loop (Fig. 1, the wire 21 creates the first node).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the first node of Blesser in the digitizer of Russell in order to have a variable loop size (as evident in Fig. 2 and 3 of Blesser.).

Yamanami et al. and Blesser also disclose a third plurality of sensing traces electrically coupled in parallel between the processor and a third node, a fourth plurality of sensing traces electrically coupled in parallel between the processor and a fourth node: a third switch coupled between one of the third plurality of sensing traces and the processor; and a fourth switch coupled between one of the fourth plurality of sensing traces and the fourth node (Please refer to the description for the first and second traces and switches above and Figure 9 and column 10, lines 28-63 of Yamanami et al. which explain that each the x and y layers shown as 81 and 82 respectively each have the configuration as that shown in Figure 1, where the first and second can be the x and the third and fourth the y.).

Yamanami et al. also disclose wherein the first array of sensing loops are each disposed at a first level but not at a different second level (Figure 9 shows that the x level loop would be at a level 81 and not at the level 82.), and wherein the second array of sensing loops are each disposed at the second level but not the first level (Figure 9 shows that the y level loop would be at a level 82 and not at the level 81.).

Yamanami et al. and Blesser fail to teach the electromagnetic digitizer sensor coupled to a processor comprising a substrate, where the first and second sensing loops are each disposed on first and second levels of the substrate respectively, and of

there being a plurality of switches to connect each of the different sensing loops to the processor or to the potential node.

Tamaru et al. disclose wherein a electronic digitizer sensor comprises a substrate, where first and second sensing electrodes are each disposed on first and second levels of the substrate respectively (Figure 7 and column 5, lines 30-63 explain that the position determining plate 10, which the examiner considers a substrate, has y electrodes on a first transparent insulating layer 11 of the substrate and x electrodes on a second transparent insulating layer 12 of the substrate.), and also disclose wherein there are a plurality of switches to connect each different sensing electrodes to the different potentials (Figure 7 shows switches 32.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switches of Tamaru et al. in the digitizer taught by the combination of Yamanami et al. and Blesser to make the sensing loops taught by Yamanami et al. and Blesser on different levels of a substrate as taught by the combination of Yamanami et al. and Blesser in order to be able to ground the sensing loops not being used for detection to reduce noise coupling of the sensing loops.

Regarding claim 12, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Tamaru et al. also disclose a sensor wherein the second node and the fourth node are each a ground node (Figure 7 shows that the node A is a ground node. And,

as explained above, since the structure on each level is the same the second and fourth nodes would each be ground nodes.).

Regarding claim 13, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses that the first node and the third node are each a floating node (Fig. 1, the node created by wire 21 is "floating" since it can commonly be used by different traces. And, as explained above, since the structure on each level is the same, then both the first and third nodes would be "floating.").

Regarding claim 14, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses the first plurality of sensing traces are disposed so as to be interleaved with the second plurality of sensing traces (It is inherent that the different plurality of traces created by Blesser's first node combined with Russell's sensing loops creates interleaved traces because Russell, Fig. 1b, shows that the lines connected to the processor alternate with the lines connected to the ground node).

Regarding claim 15, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses a sensor wherein the first plurality of switches are embodied as a multiplexor (Figure 1 shows that the switches 17-1 through 17-10 are in a multiplexor 19 [see column 5, lines 31-34].).

Regarding claim 16, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Tamaru et al. also discloses a sensor wherein the first plurality of sensing traces are further switchably connectable to the second node and the second plurality of sensing traces are further switchably connectable to the processor, the third plurality of sensing traces are further switchably connectable to the fourth node, and the fourth plurality of sensing traces are further switchably connectable to the processor (The switches 32 allow each trace in Tamaru et al. to be connected to either a second node or the voltage source, which is the equivalent of the processor in Yamanami et al. And, as explained above, since the structure on each level is the same, then both the third and fourth traces would mirror the first and second.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the further teachings of Tamaru et al. in the sensor taught by the combination of Yamanami et al., Blesser and Tamaru et al., in order to have each trace act as a connection to the source or the ground.

Regarding claim 17, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses a sensor wherein the first and second plurality of sensing traces are arranged in a comb-like pattern (It is inherent that the different plurality of traces created by Blesser's first node combined with Russell's sensing loops creates a comb-like pattern as in Blesser Fig. 1).

Regarding claim 18, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses a sensor wherein the first and second plurality of sensing traces are each arranged to be physically parallel with each other, and the third and fourth plurality of sensing traces are each arranged to be physically parallel with each other. (It is inherent that the different plurality of traces created by Blesser's first node combined with Yamanami et al.'s sensing loops creates traces that are each arranged to be physically parallel with each other. And, as explained above, since the structure on each level is the same, then both the third and fourth traces would mirror the first and second.).

Regarding claim 19, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses a sensor wherein the first and second plurality of switches are each single-pole-single-throw switches (Fig. 1, switches 17-1).

Regarding claims 20 and 21, Yamanami et al., Blesser and Tamaru et al. disclose the electromagnetic digitizer sensor of claim 11.

Blesser also discloses a sensor wherein the first, second, third and fourth pluralities of sensing traces form conductive loops that are variable in both size and position depending upon states of the third and fourth plurality of switches (Figures 1-3 show that by closing a different switch the size of the loop and the position at which is starts are both changed. And, as explained above, since the structure on each level is the same, then both the third and fourth traces would mirror the first and second.).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chao et al. (US 2004/0174343) disclose a multi-channel switches set produced in semiconductor processes to replace traditional analog switch and tri-state element used in prior art as signal transmitting/receiving selector of inductor loops of a tablet, which can simplify the controlling circuit, enhance power efficiency of signal transmitting/receiving between the tablet system and a cord less and cell less pointer apparatus, and increase speed of the response of signal transmitting/receiving between the tablet and a cord less-battery less pointer apparatus.

Chao et al. (US 2004/-0130534) disclose a plurality of single-induction-loops that are inserted in an electromagnetic induction system in which multi-induction-loops are deployed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

4 January 2007

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SUPERVISORY PATENT EXAMINER